AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

Claims 1–27 (cancelled).

28. (previously presented) A chemical-mechanical polishing process, comprising the steps of:

forming a first conductive layer and a dielectric layer over a semiconductor substrate;

polishing the dielectric layer to form a substantially planar surface; and

forming a dielectric cap layer over the dielectric layer.

29. (previously presented) The process of claim 28, wherein the step of forming the conductive layer includes depositing doped polysilicon.

30. (previously presented) The process of claim 28, wherein the step of forming the dielectric layer includes a high-density plasma chemical vapor deposition method.

31. (previously presented) The process of claim 28, wherein the step of forming the dielectric layer includes depositing silicon dioxide.

32. (currently amended) The process of claim 28, wherein the step of forming the dielectric layer includes ~~depositing silicon dioxide~~ a plasma enhanced chemical vapor deposition method.

33. (previously presented) The process of claim 28, wherein the step of forming the cap layer includes depositing a silicon oxide layer using a plasma-enhanced chemical vapor deposition method with silane (SiH_4) as the main reactive agent.

34. (previously presented) The process of claim 28, wherein the silicon oxide layer is deposited to a thickness of about 1000-3000 Angstroms and can be adjusted according to design rules.

35. (previously presented) The process of claim 28, wherein the step of forming the cap layer includes depositing a silicon oxide layer using a chemical vapor

deposition method with tetra-ethyl-ortho-silicate (TEOS) as the main reactive agent.

36. (previously presented) The process of claim 28, wherein the silicon oxide layer is deposited to a thickness of about 1000-3000 Angstroms and can be adjusted according to design rules.

37. (previously presented) The process of claim 28, wherein the step of forming the cap layer includes depositing a silicon nitride layer using a chemical vapor deposition method with silane (SiH_4) as the main reactive agent.

38. (previously presented) The process of claim 28, wherein the silicon nitride layer is deposited to a thickness of about 100-3000 Angstroms and can be adjusted according to design rules.

39. (previously presented) The process of claim 28, wherein the step of forming the cap layer includes depositing a silicon nitride layer using a chemical vapor deposition method with silicon dichlorohydride (SiH_2Cl_2) as the main reactive agent.

40. (previously presented) The process of claim 28, wherein the silicon nitride layer is deposited to a thickness of about 100-3000 Angstroms and can be adjusted according to design rules.

41. (previously presented) The process of claim 28, wherein the step of forming the cap layer includes depositing silicon dioxide.

42. (previously presented) The process of claim 28, wherein the step of forming the cap layer includes depositing phosphosilicate glass (PSG).

43. (previously presented) The process of claim 28, wherein the step of forming the cap layer includes depositing silicon-rich oxide (SRO).

44. (previously presented) A process of forming a conductive interconnect, the process comprising the steps of:

providing a semiconductor substrate having a conductive layer thereon;

forming a dielectric layer over the substrate and the conductive layer;

polishing the surface of the dielectric layer to form a substantially planar surface; and

forming a dielectric cap layer over the dielectric layer.

45. (previously presented) A chemical mechanical polishing process, comprising the steps of:

(a) forming a conductive layer over a semiconductor substrate; and

(b) patterning said conductive layer to form interconnect lines;

(c) forming at least one dielectric layer over said interconnect lines, said at least one dielectric layer having a first thickness;

(d) polishing said at least one dielectric layer to form a planar surface; and

(e) forming a thin cap layer over said planar surface, said thin cap layer having a second thickness which is sufficient to fill scratches formed in said at least one dielectric layer during said polishing step (d), and which second thickness is substantially less than said first thickness.

46. (previously presented) The method of claim 45 wherein said first thickness is about 20K Angstroms to 30K Angstroms, and said second thickness is about 1K to 3K Angstroms.

47. (previously presented) The method of claim 45, wherein said first thickness is about ten times greater than said second thickness.

48. (previously presented) The method of claim 45, wherein said cap layer prevents metal bridges from forming in said scratches of said at least one dielectric layer.

49. (previously presented) The method of claim 45, wherein said at least one dielectric layer includes a fluorinated silicon glass (FSG) layer.

50. (previously presented) The method of claim 45, wherein said at least one dielectric layer further includes a high density plasma chemical vapor deposition layer formed between and over said interconnect lines.

51. (previously presented) The method of claim 45, wherein said cap layer includes silicon oxide, silicon nitride, phosphosilicate glass (PSG), and/or silicon-rich oxide.

52. (previously presented) The method of claim 45, wherein said conductive layer includes doped polysilicon.

53. (previously presented) The method of claim 45, wherein said cap layer provides a higher degree of surface planarity than said planar surface, and further forms a highly planar surface that can reduce undesirable diffractions from height differences so that during a subsequent photolithographic operation undesirable diffractions from height differences are reduced.

54. (previously presented) The method of claim 45, wherein said further including the steps of:

patterning said cap layer and said at least one dielectric layer to form openings to said conductive layer;

forming an additional conductive layer over said cap layer and in said openings, such that conductive vias are formed between said conductive layer and said additional conductive layer;

patterning said additional conductive layer to form additional interconnects over said cap layer.

55. (previously presented) A chemical mechanical polishing process, comprising the steps of:

(a) forming a conductive layer over a semiconductor substrate;

(b) patterning said conductive layer to form interconnect lines;

(c) forming at least one dielectric layer over said interconnect lines, said at least one dielectric layer having a first thickness;

(d) polishing said at least one dielectric layer to form a polished surface; and

(e) forming a thin cap layer over said polished surface to planarize said polished surface, said thin cap layer having a second thickness which is substantially less than said first thickness.

56. (previously presented) The method of claim 55 wherein said first thickness is about 20K Angstroms to 30K Angstroms, and said second thickness is about 1K to 3K Angstroms.

57. (previously presented) The method of claim 55, wherein said first thickness is about ten times greater than said second thickness.

58. (previously presented) The method of claim 55, wherein said cap layer prevents metal bridges from forming in said scratches of said at least one dielectric layer.

59. (previously presented) The method of claim 55, wherein said at least one dielectric layer includes a fluorinated silicon glass (FSG) layer.

60. (previously presented) The method of claim 55, wherein said at least one dielectric layer further includes a high density plasma chemical vapor deposition layer formed between and over said interconnect lines.

61. (previously presented) The method of claim 55, wherein said cap layer includes silicon oxide, silicon nitride, phosphosilicate glass (PSG), and/or silicon-rich oxide.

62. (previously presented) The method of claim 55, wherein said conductive layer includes doped polysilicon.

63. (previously presented) The method of claim 55, wherein said cap layer provides a higher degree of surface planarity than said planar surface, and further forms a highly planar surface that can reduce undesirable diffractions from height differences so that during a subsequent photolithographic operation undesirable diffractions from height differences are reduced.

64. (previously presented) The method of claim 55, wherein said further including the steps of:

patterning said cap layer and said at least one dielectric layer to form openings to said conductive layer;

forming an additional conductive layer over said cap layer and in said openings, such that conductive vias are formed between said conductive layer and said additional conductive layer;

patterning said additional conductive layer to form additional interconnects over said cap layer.